AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells which are slower in a write operation than in a read operation; and

a cache memory for mediating an access to said plurality of memory banks from the outside,

said cache memory having a number of ways equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells;

wherein, when first data is written into said semiconductor device from the outside, and when said cache memory does not hold a first address at which said first data is to be written, second data held in an entry associated with the first address of said cache memory is written back to one of said plurality of memory banks, and said first data is written into said cache memory, and

wherein, when ~~this~~ third data is written into said semiconductor device from the outside when the second data is written back to one of said plurality of memory banks and said cache memory does not hold a second address at which said third data is to be written, fourth data held in an entry associated with the second address is written back to a second memory bank, different from the first memory bank, included in said plurality of memory banks.

2. (original) A semiconductor device according to claim 1, wherein:

said cache memory has a plurality of sets corresponding to the number of ways, and

each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks.

3. (original) A semiconductor device according to claim 1, wherein:

when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory.

Claim 4 (canceled).

Claim 5 (Canceled).

6. (original) A semiconductor device according to claim 1, further comprising:

a plurality of data input/output nodes for inputting/outputting data to/from the outside,

wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device.

7. (original) A semiconductor device according to claim 1, further comprising:

an internal data bus for coupling said cache memory to said memory banks; and

a plurality of data input/output nodes for inputting/outputting data from/to the outside,

wherein said cache memory has a cache line comprised of a plurality of sublines, and

$$A = N \cdot B$$

is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus.

8. (original) A semiconductor device according to claim 7, wherein:

said cache memory has a plurality of flags each associated with one subline for managing data held thereon; and

when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank.

9. (Previously Presented) A semiconductor device according to claim 7, wherein:

when a flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory.

10. (original) A semiconductor device according to claim 1, wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or an phase change memory cell.

11. (original) A semiconductor device according to claim 10, wherein said cache memory comprises SRAM memory cells.

12. (original) A semiconductor device according to claim 1, wherein said cache memory comprises SRAM memory cells.

Claims 13 through 19 (canceled).

20. (Previously Presented) A semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells which are slower in a write operation than in a read operation; and

a cache memory for mediating an access to said plurality of memory banks from the outside,

said cache memory having a number of ways equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells;

an internal data bus for coupling said cache memory to said memory banks; and

a plurality of data input/output nodes for inputting/outputting data from/to the outside,

wherein said cache memory has a cache line comprised of a plurality of sublines, and

$$A = N \cdot B$$

is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus,

wherein, when first data held in said cache memory is written back to one of said plurality of memory banks, and when a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to a write back operation to write second data held in said cache memory, the first data is written back to a second memory bank, different from the first memory bank, included in said plurality of memory banks.

21. (Previously Presented) A semiconductor device according to claim 20, wherein:

said cache memory has a plurality of sets corresponding to the number of ways, and

each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks.

22. (Previously Presented)A semiconductor device according to claim 20, wherein:

when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory.

23. (Previously Presented) A semiconductor device according to claim 20, further comprising:

a plurality of data input/output nodes for inputting/outputting data to/from the outside,

wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device.

24. (Previously Presented) A semiconductor device according to claim 20, wherein:

said cache memory has a plurality of flags each associated with one subline for managing data held thereon; and

when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank.

25. (Previously Presented) A semiconductor device according to claim 20, wherein:

when a flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory.

26. (Previously Presented) A semiconductor device according to claim 20, wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or an phase change memory cell.

27. (Previously Presented) A semiconductor device according to claim 26, wherein said cache memory comprises SRAM memory cells.

28.(Previously Presented) A semiconductor device according to claim 20, wherein said cache memory comprises SRAM memory cells.